

PTO/SB/122 (04-05)

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Application Number	10,728,036
Filing Date	December 3, 2003
First Named Inventor	Cam L. Lu et al.
Art Unit	2825
Examiner Name	Siek, Vuthe
Attorney Docket Number	03-1978 / 81641

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Signature

Timothy Croll

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Timothy Croll, Reg. No. 36,771

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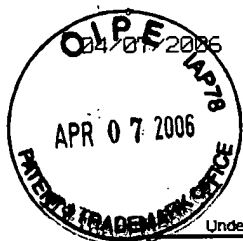
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NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

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PTO/SB/06 (08-03)

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STATEMENT UNDER 37 CFR 3.73(b)Applicant/Patent Owner: LSI Logic CorporationApplication No./Patent No.: 10,728,036 Filed/Issue Date: December 3, 2003Entitled: Method of Generating an Efficient Stuck-At Fault and Transition Delay Fault Truncated Scan Test Pattern for an Integrated Circuit DesignLSI LOGIC CORPORATION, a CORPORATION

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest; or
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[NOTE: A separate copy (i.e., the original assignment document or a true copy of the original document) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

7 APR 06
Date
(408) 433-7191
Telephone number

Timothy Croll, Reg. No. 36,771
Typed or printed name
[Signature]
Signature
Sr. Corporate Counsel - IP
Title

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